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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/841,582	04/24/2001	Kazuo Nishiyama	09792909-4979	5398

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EXAMINER	
ZARNEKE, DAVID A	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 11/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/841,582	NISHIYAMA ET AL.	
	Examiner	Art Unit	
	David A. Zarneke	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 6-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 6-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 10/2/06, with respect to the rejections of claims 6-9 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Wolf, Silicon Processing for the VLSI Era, Volume 2:Process Integration, 1990, pp 334, 335 & 337.

It is argued, and agreed with by the examiner, that that art of record fails to teach the use of a silicon dioxide layer between the chip and the passivation layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Camien et al., US Patent 5,953,588, in view of Wolf, Silicon Processing for the VLSI Era, Volume 2:Process Integration, 1990, pp 334, 335 & 337.

Camien (figure 5 & 6) teaches a pseudo wafer comprising a plurality of semiconductor chips [106] each having at least their electrodes formed solely on one surface thereof (6, 33-36), wherein interspaces between each individual one of said chips and bottom surfaces thereof are continuously covered with said protective material [104], and the chips are bonded with each other via the protective material, there being substantially none of the protective material formed on the one surface at which the electrodes are formed (figure 6 & 6, 33-36).

Camien, which teaches performing "desired steps" on the active surface of the dies, fails to teach the electrodes being covered with a solder material for forming a solder ball.

It would have been obvious to one of ordinary skill in the art at the time of the invention to cover the electrodes with a solder material in order to form a solder ball because solder ball formation is a conventional, well-known in the art step to perform on exposed electrodes. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

Further, Camien fails to teach the use of a silicon dioxide layer formed over the one surface at which the electrodes are formed and a passivation layer formed over the silicon dioxide having openings at locations corresponding to the electrodes.

Wolf (pp 334-335 and Figure 5-16 on pp 337) teaches the use of a silicon dioxide layer formed over the one surface at which the electrodes are formed and a passivation layer formed over the silicon dioxide having openings at locations corresponding to the electrodes.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the silicon dioxide layer of Wolf in the invention of Camien because Wolf teaches this layer insulates the chip form the metal electrode, reduces the parasitic capacitance of the interconnect metallization layer, acts as a NA+ getter, and produces better step coverage (p 335, 1st full paragraph).

Regarding claim 7, Camien teaches the protective material comprises either one of an organic insulating resin and an inorganic insulating material in teaching that the material can be an epoxy (6, 24+).

With respect to claim 8, Camien teaches the plurality of semiconductor chips arrayed thereon are diced at a position of said protective material between said plurality

of semiconductor chips and thereafter mounted on a packaging substrate such that the protective material adjacent the side surfaces of the semiconductor chip is cut to provide substantially vertical side walls of protective material formed adjacent the sides of the semiconductor chip (6, 37+).

As to claim 9, while Camien fails to teach a solder bump is formed on said electrode, it would have been obvious to one of ordinary skill in the art at the time of the invention to cover the electrodes with a solder bump because solder bumps are a conventional, well-known in the art step to perform on exposed electrodes. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paik et al., US Patent 5,879,964, in view of Wolf, Silicon Processing for the VLSI Era, Volume 2:Process Integration, 1990, pp 334, 335 & 337.

Paik (figure 5a) teaches a pseudo wafer comprising a plurality of semiconductor chips each having at least their electrodes formed solely on one surface thereof, wherein interspaces between said chips and bottom surfaces thereof are continuously covered with said protective material, and the chips are bonded with each other and further wherein the protective material adjacent the side surfaces of each semiconductor chip is cut to provide substantially vertical side walls of protective material formed adjacent the sides of the semiconductor chips.

While Paik teaches using wafer strips comprising several dice as opposed to the presently claimed individual dice, it would have been obvious to one of ordinary skill in the art at the time of the invention to use an individual die as opposed to the wafer strip

of Paik because the omission of an element (in this case the extra chips) with a corresponding omission of its function is within the level of ordinary skill in the art (In re Wilson 153 USPQ 740 (CCPA 1967); In re Portz 145 USPQ 397 (CCPA 1965); In re Larson 144 USPQ 347 (CCPA 1965); In re Karlson 136 USPQ 184 (CCPA 1963); In re Listen 58 USPQ 481 (CCPA 1943); In re Porter 20 USPQ 298 (CCPA 1934)).

Further, Paik fails to teach the use of a silicon dioxide layer formed over the one surface at which the electrodes are formed and a passivation layer formed over the silicon dioxide having openings at locations corresponding to the electrodes.

Wolf (pp 334-335 and Figure 5-16 on pp 337) teaches the use of a silicon dioxide layer formed over the one surface at which the electrodes are formed and a passivation layer formed over the silicon dioxide having openings at locations corresponding to the electrodes.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the silicon dioxide layer of Wolf in the invention of Paik because Wolf teaches this layer insulates the chip form the metal electrode, reduces the parasitic capacitance of the interconnect metallization layer, acts as a NA+ getter, and produces better step coverage (p 335, 1st full paragraph).

In re claim 7, Paik teaches the protective material comprises an epoxy (4, 21+), either is one of an organic insulating resin and an inorganic insulating material.

Regarding claim 8, Paik teaches the plurality of semiconductor chips arrayed thereon are diced at a position of said protective material between said plurality of semiconductor chips and thereafter mounted on a packaging substrate such that the

protective material adjacent the side surfaces of the semiconductor chip is cut to provide substantially vertical side walls of protective material formed adjacent the sides of the semiconductor chip.

With respect to claim 9, Paik teaches a solder bump [9] formed on said electrode.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication from the examiner should be directed to David A. Zarneke whose telephone number is (571)-272-1937. The examiner can normally be reached on M-Th 7:30 AM-6 PM. If attempts to reach the examiner are

unsuccessful, the examiner's supervisor, William Baumeister can be reached on (571)-272-1722. The fax phone number where this application is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

David A. Zarneke
Primary Examiner
November 24, 2006